New approaches to classical Silicon Solar Cells

The SSTEP Project

Solar-grade Silicon by Transfer and EPitaxy

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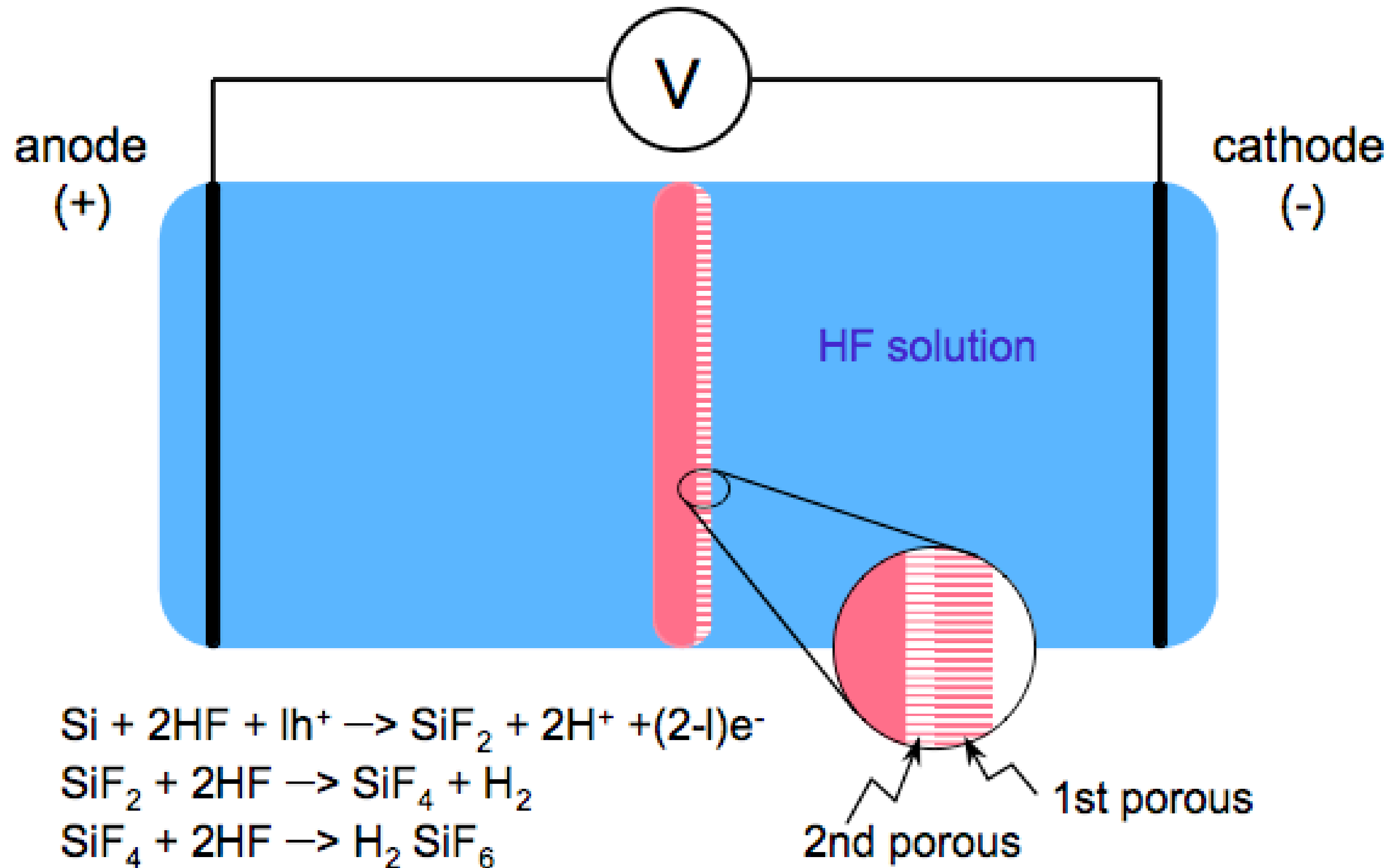
What's the porous Si ?

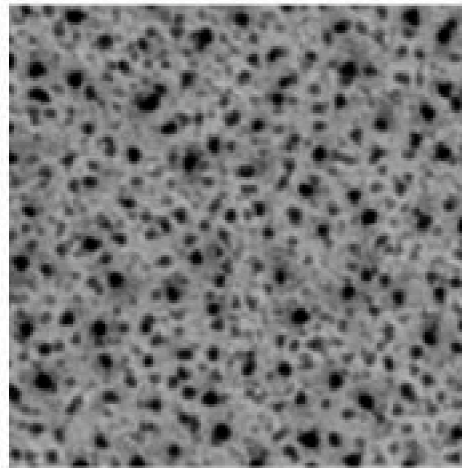
Principle of anodization reaction



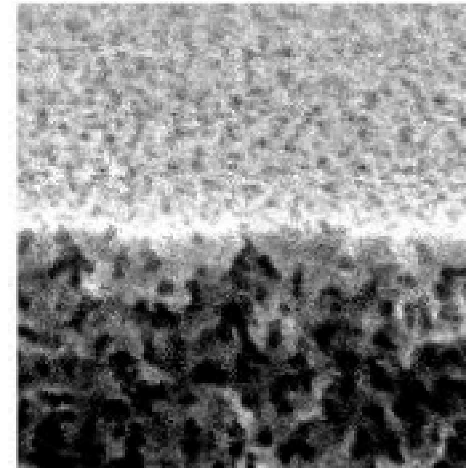
Porous structure

SEM images

plan-view



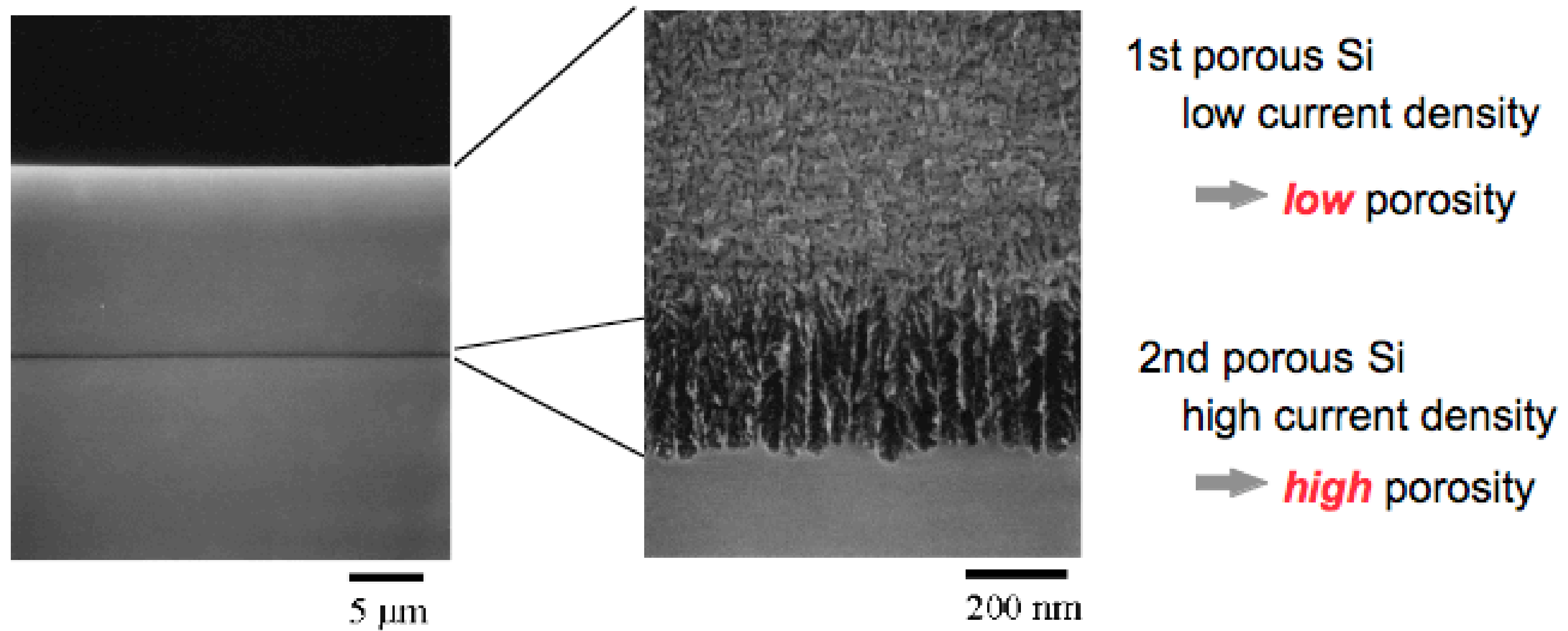
oblique-view



100nm

Pore size 6~8 nm, pitch 10~30 nm
Pore density ~ 10^{11} cm^{-2}, Porosity ~20%

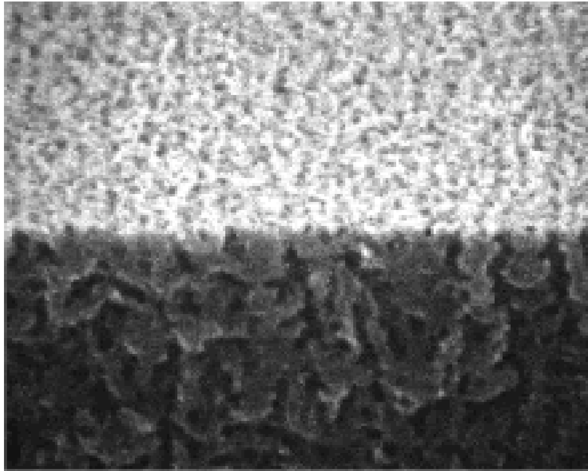
porous Si layer



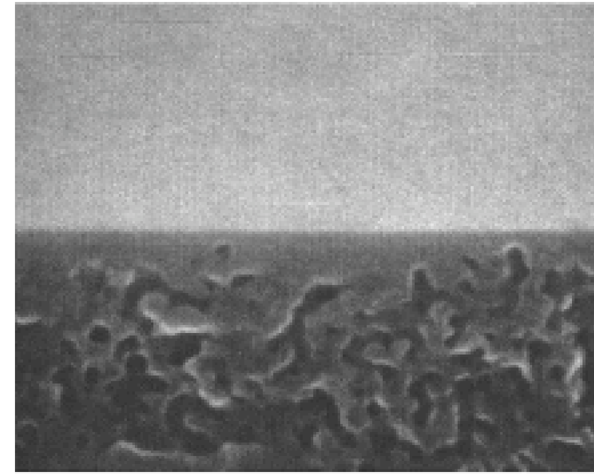
restructured porous Si

Just before Epi !

oblique-view



as-anodized



pre-baked in epi chamber

Epitaxy

- CVD is the most common method of Si epitaxy

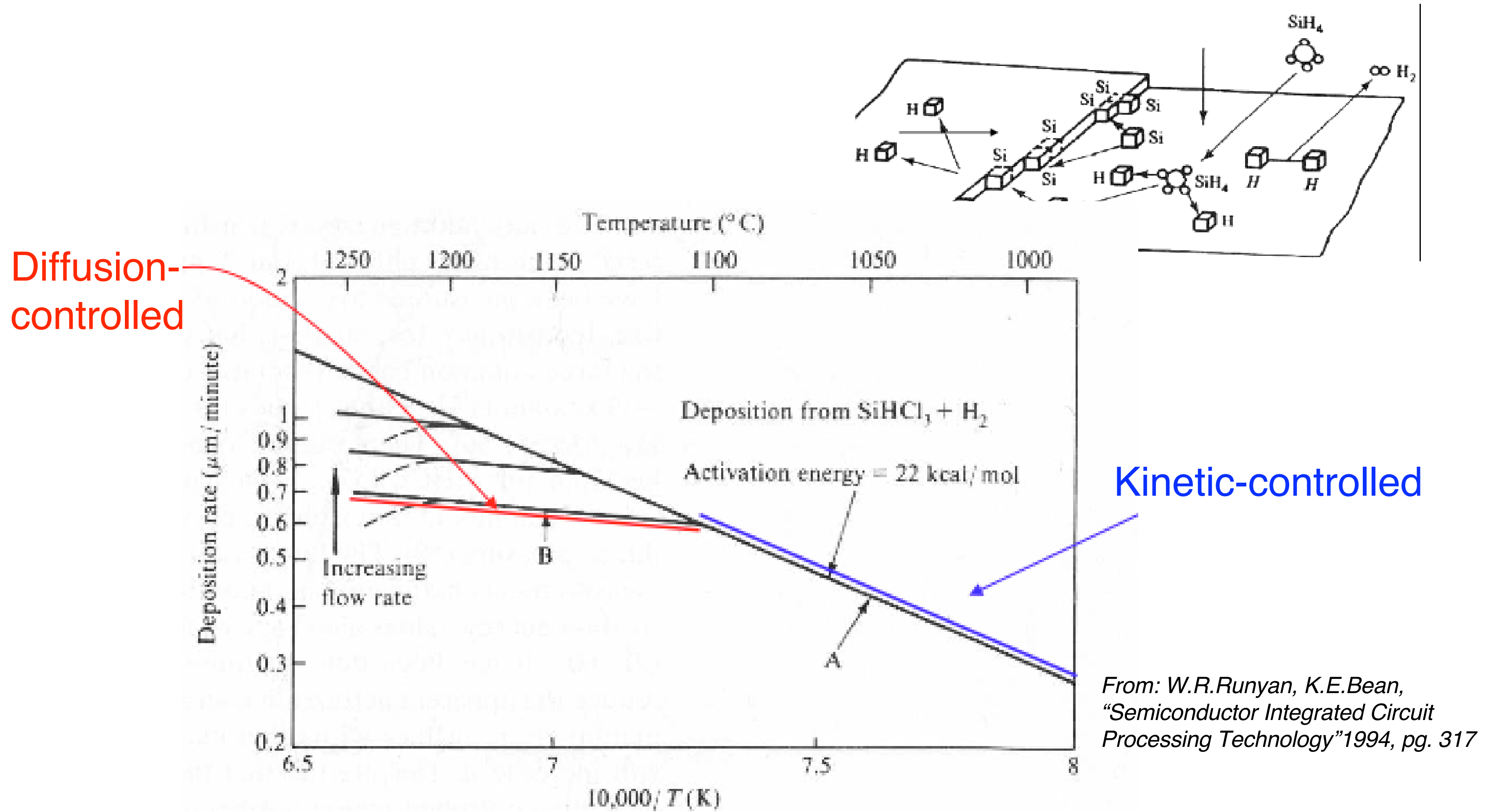
- Reduction of chlorosilanes($SiCl_4$, $SiHCl_3$, SiH_2Cl_2, SiH_4) at high temperature (~ 900 °C -1150 °C),
e.g.– $SiHCl_3$ (v) + H_2(v) Si (s) + 3HCl (v)

- Hydrogen is used as reducing agent and carrier gas.

- The reaction is surface catalyzed.
- $SiHCl_3$and SiH_2Cl_2 are typical silicon sources– Good balance between safety and process needs in atmospheric conditions–

Today, TCS is the preferred source (liquid at RT) requires medium high deposition temperature – $SiCl_4$requires too high deposition temperature – SiH_4 is used when a low transition region or no pattern shift is requested. Very low deposition temp (900 °C) but more difficult to manage than TCS.

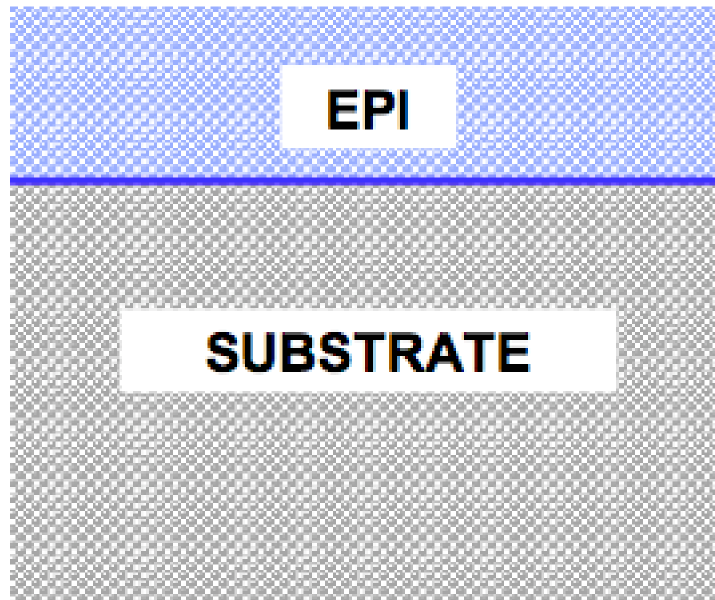
Epitaxy



From: W.R.Runyan, K.E.Bean, "Semiconductor Integrated Circuit Processing Technology"1994, pg. 317

Epitaxy

Doping The dopant is co-deposited with silicon.



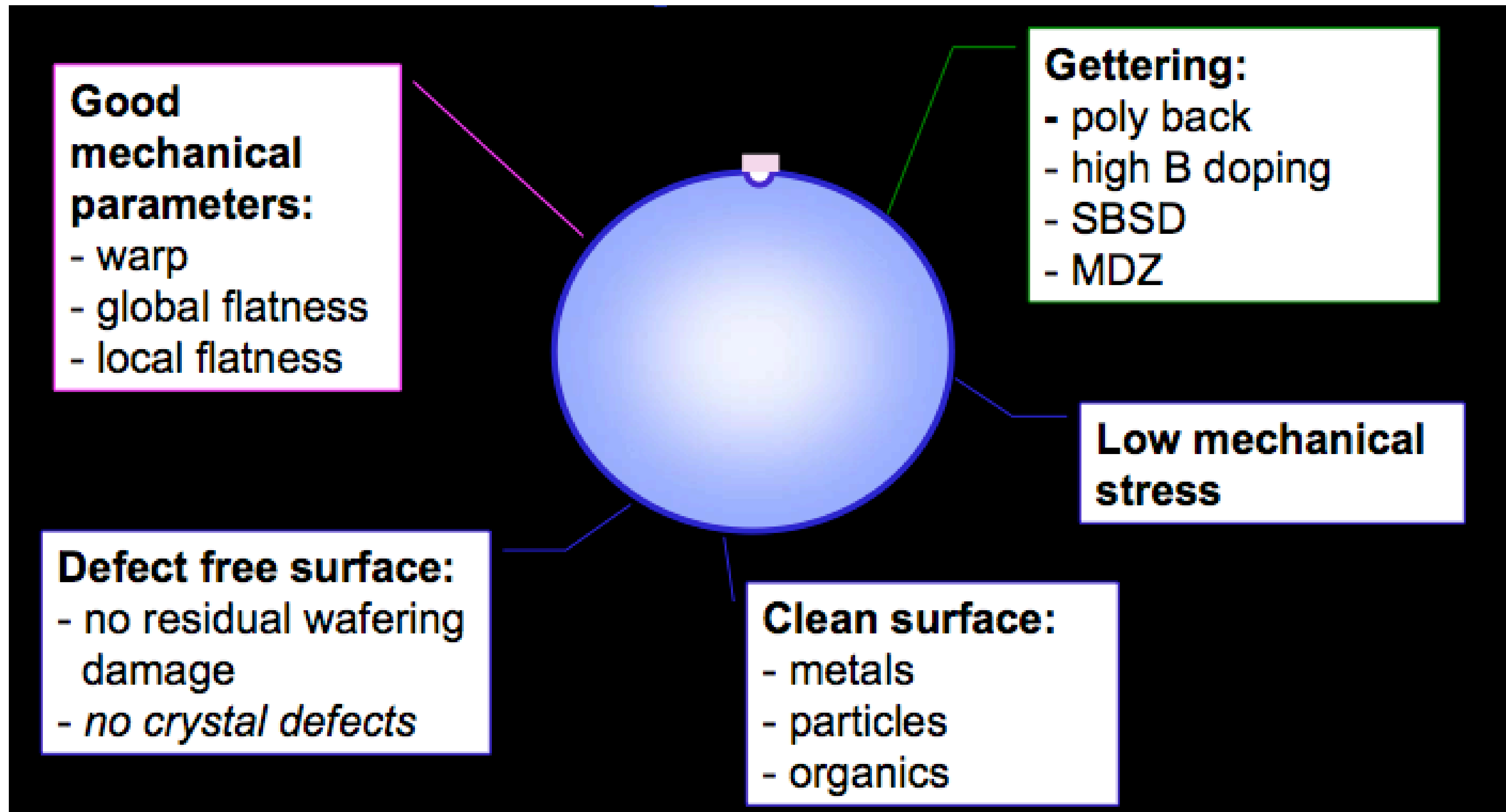
Epi dopant and resistivity:

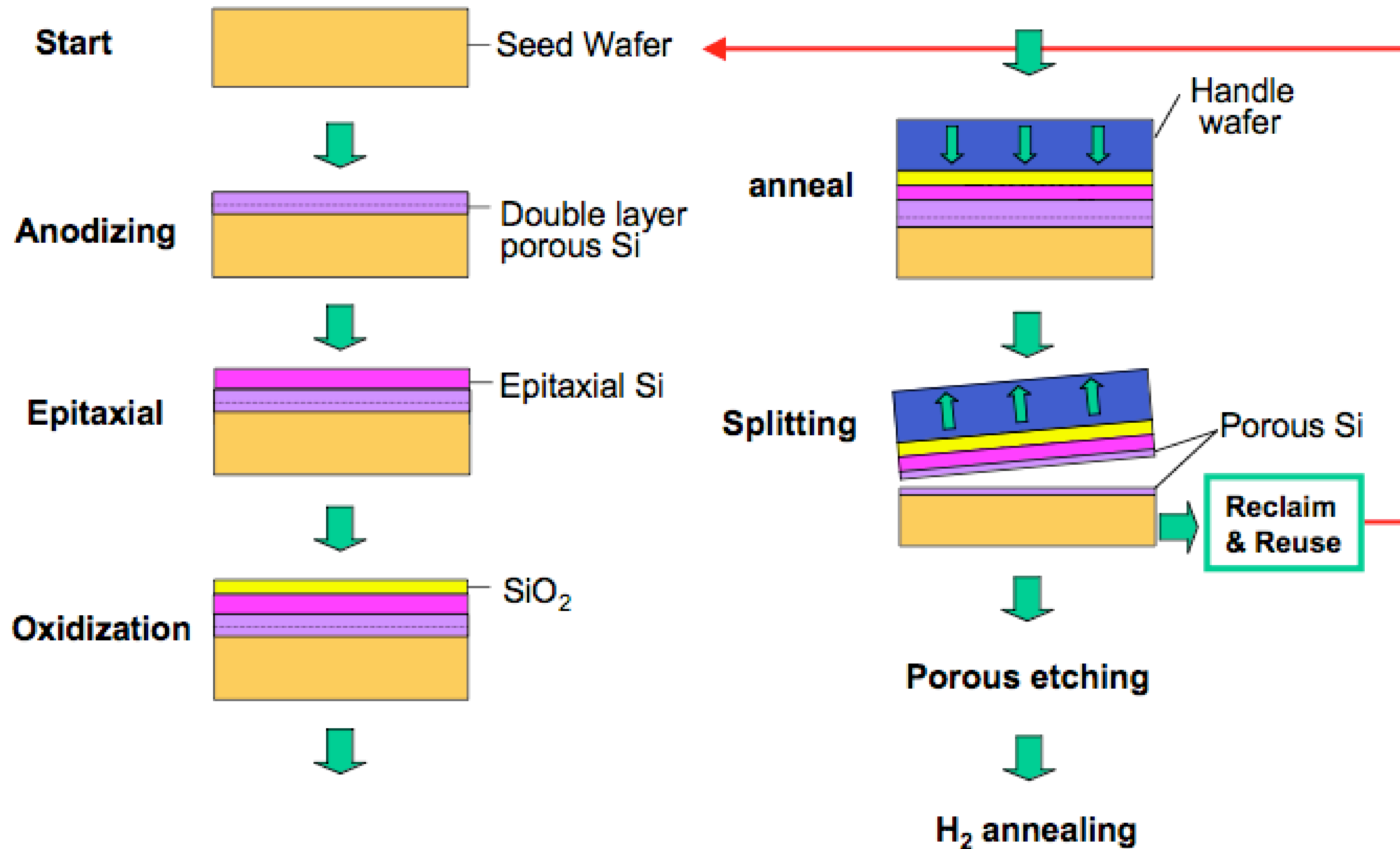
- *type P:* B (B2H6) -> 0.1 -100 ohm*cm
- *type N:* P (PH 3) As (AsH 3) 0.03 - 50 Ωcm

Substrate dopant and resistivity:

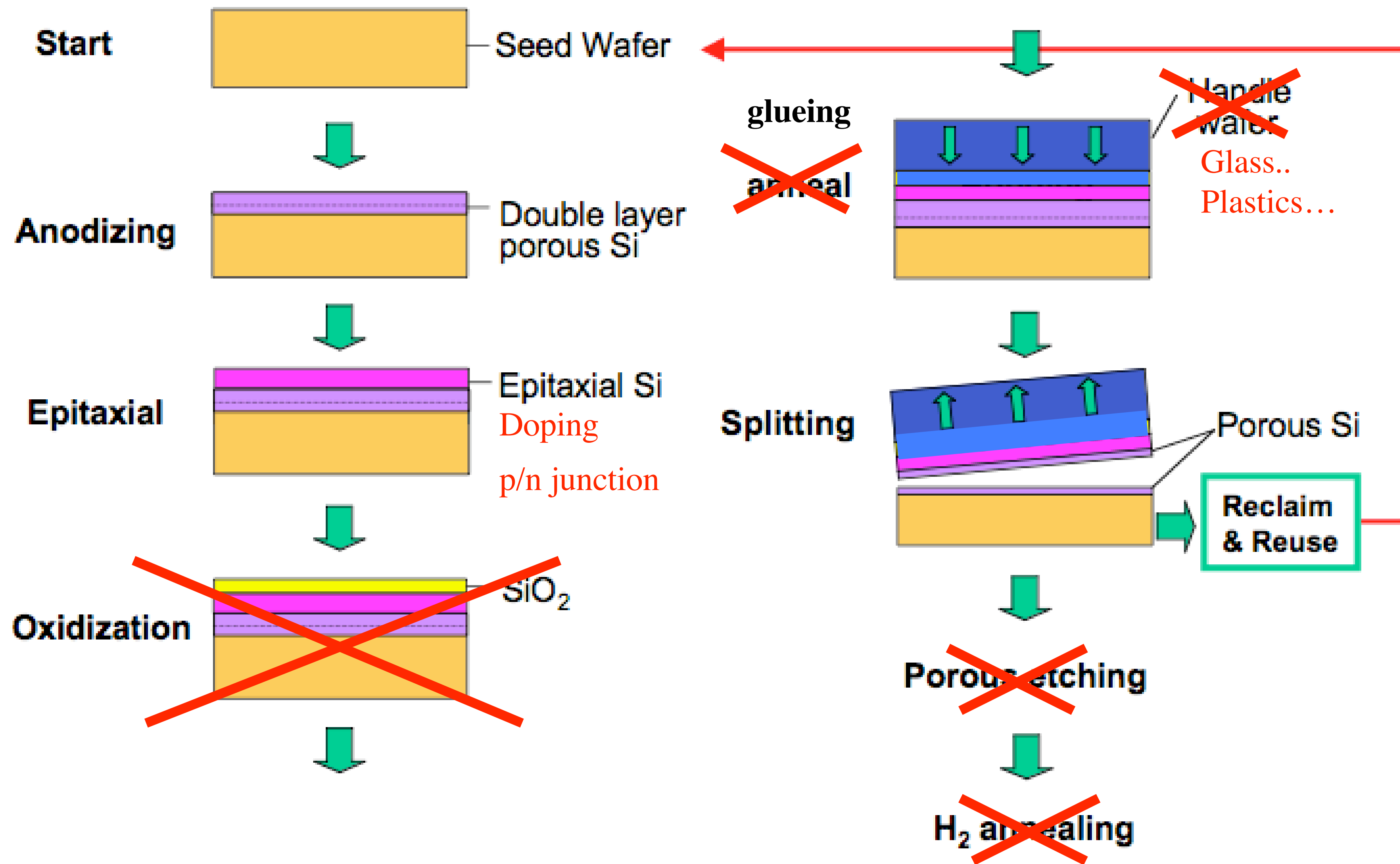
- *type P++*: B -> 2-5 mohm*cm
- *type P+*: B -> 8 -20 mohm*cm
- *type P-*: B -> >1 ohm*cm
- *type N++:* As,Red-P ->1-5 mohm*cm
- *type N+*: Sb-> 15 -30 mohm*cm

Epitaxy

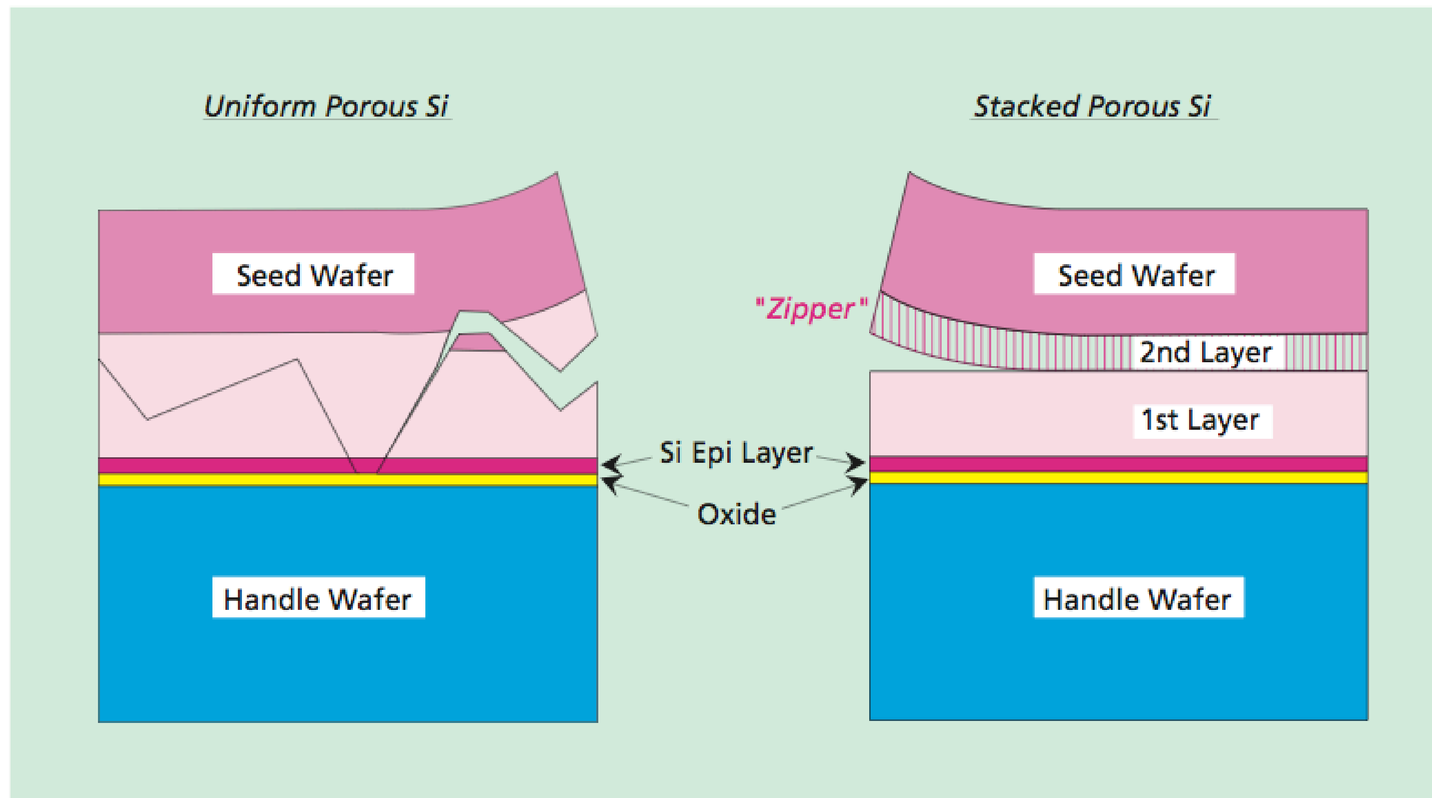



ELTRAN fabrication process
Start
Seed Wafer
Anodizing
Double layer porous Si
Epitaxial
Epitaxial Si
Oxidization
SiO_2
anneal
Handle wafer
Splitting
Porous Si
Reclaim & Reuse
Porous etching
H_2 annealing

SSTEP fabrication process



SSTEP



SSTEP

the ***'seed wafer reusage'*** concept

$$Y = H + \frac{S + R \cdot (n-1)}{n}$$

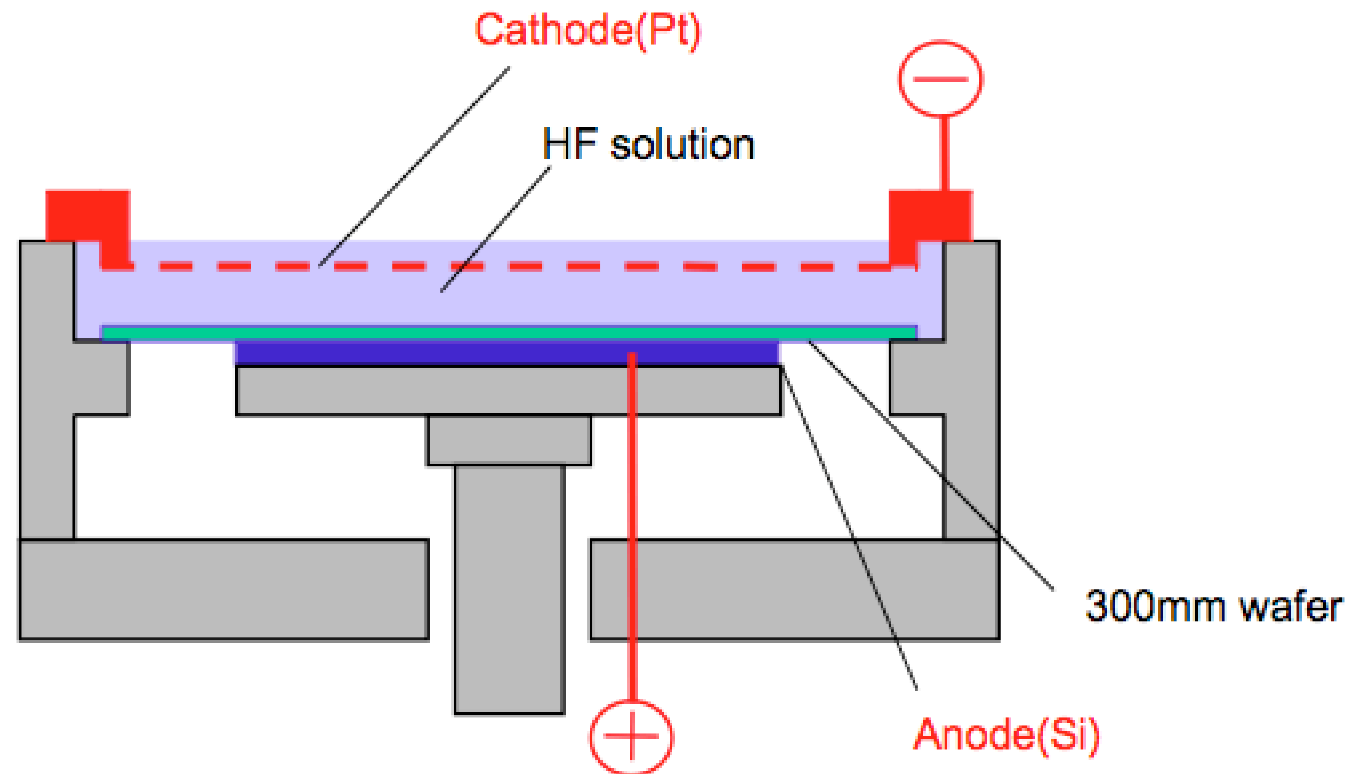
Y is the SSTEP wafer cost
H is the price of the handle substrate
S is the price of the seed wafer
R is the price of reclaiming the seed wafer
N is the number of times the seed wafer is re-used

As n increases…

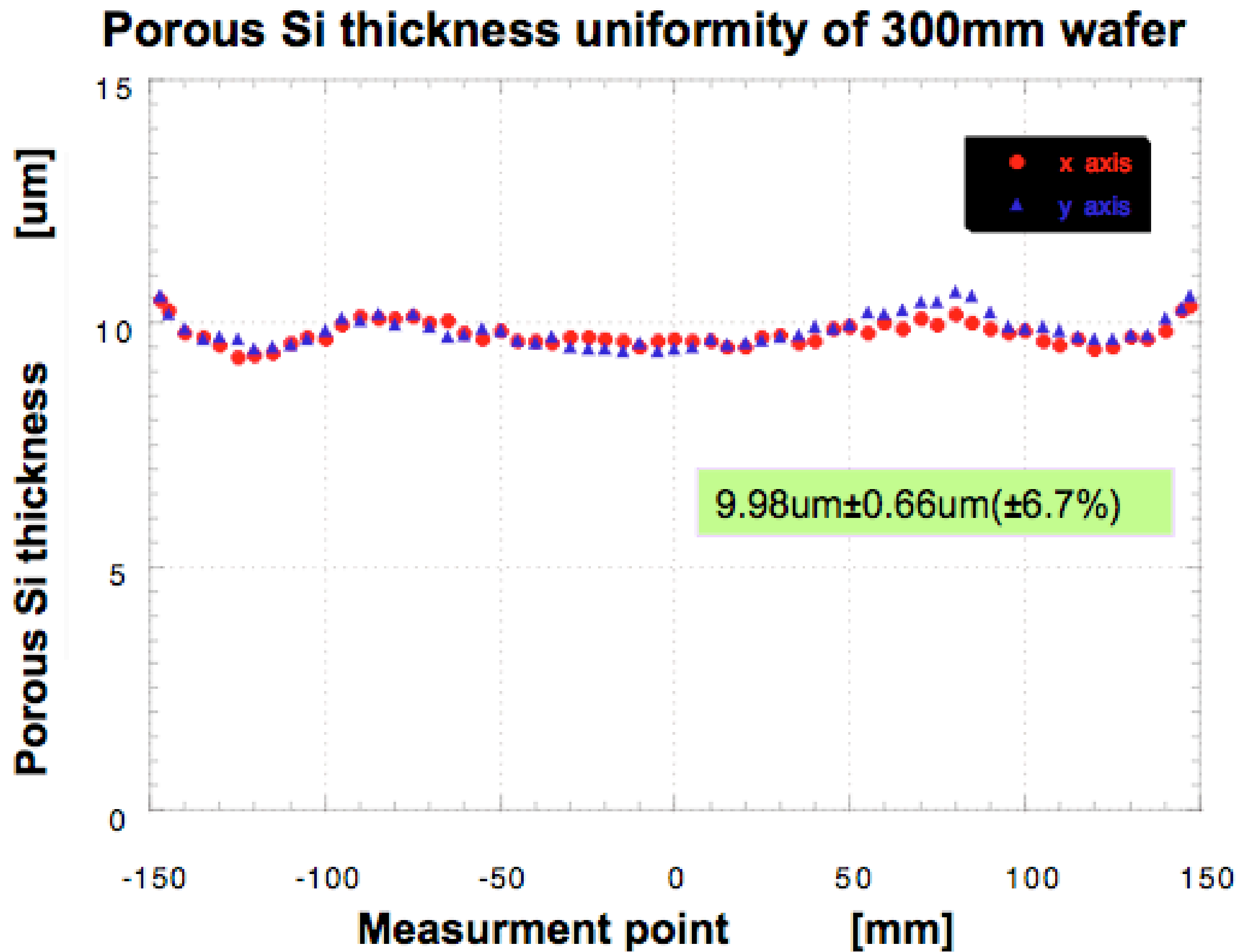
$$Y \to H + R$$

300mm anodization apparatus

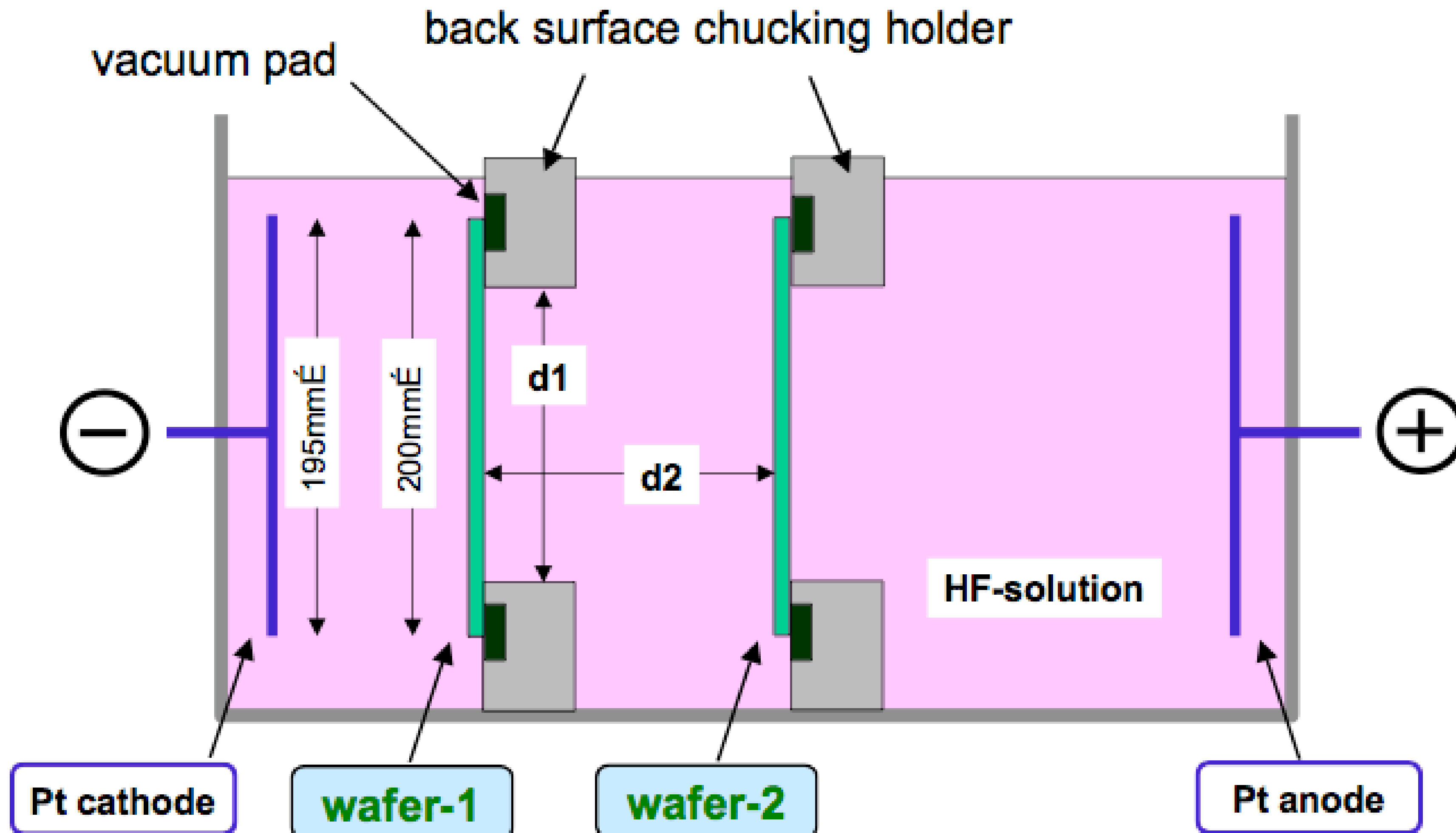
Single wafer processing type



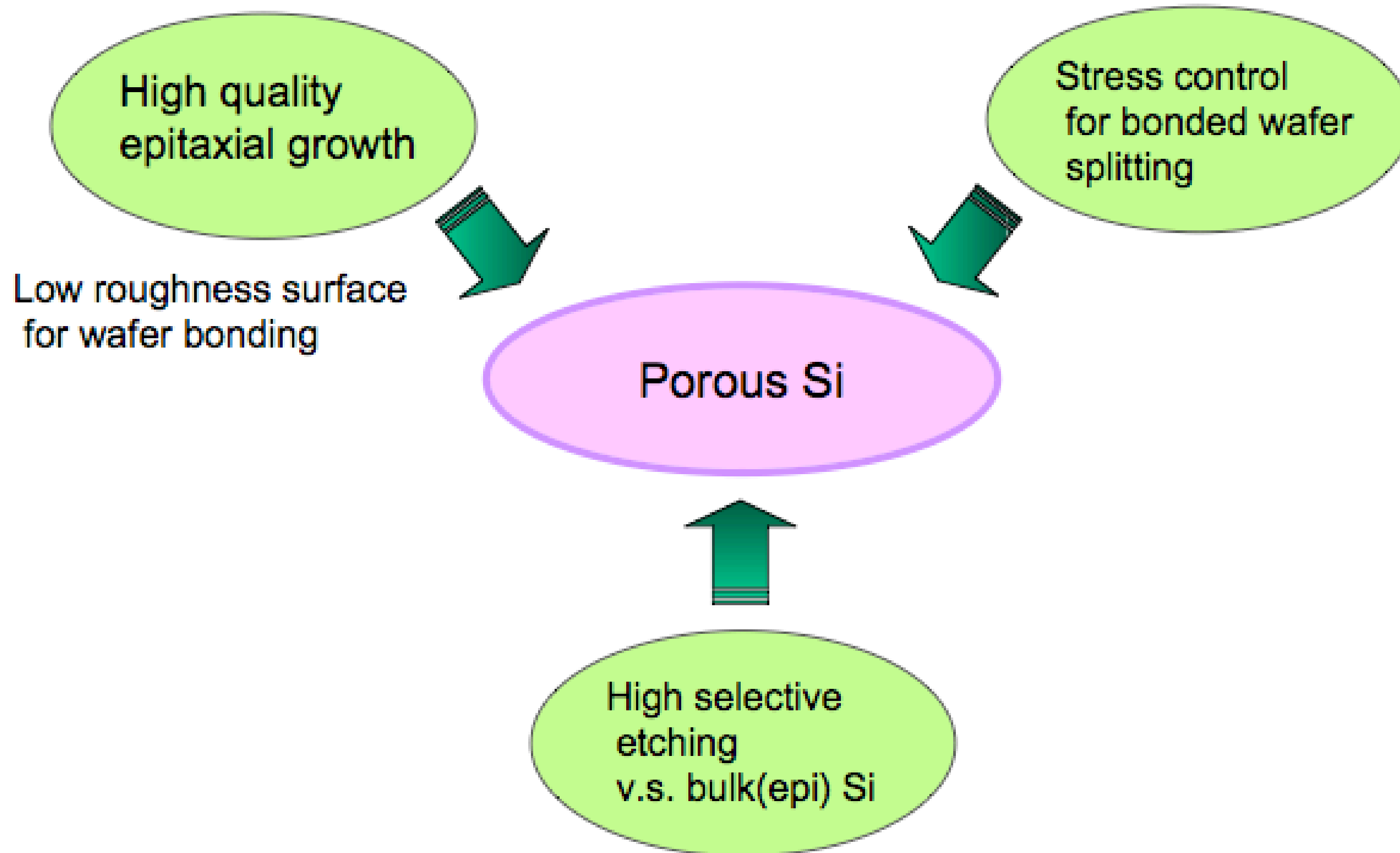
300mm porous Si thickness



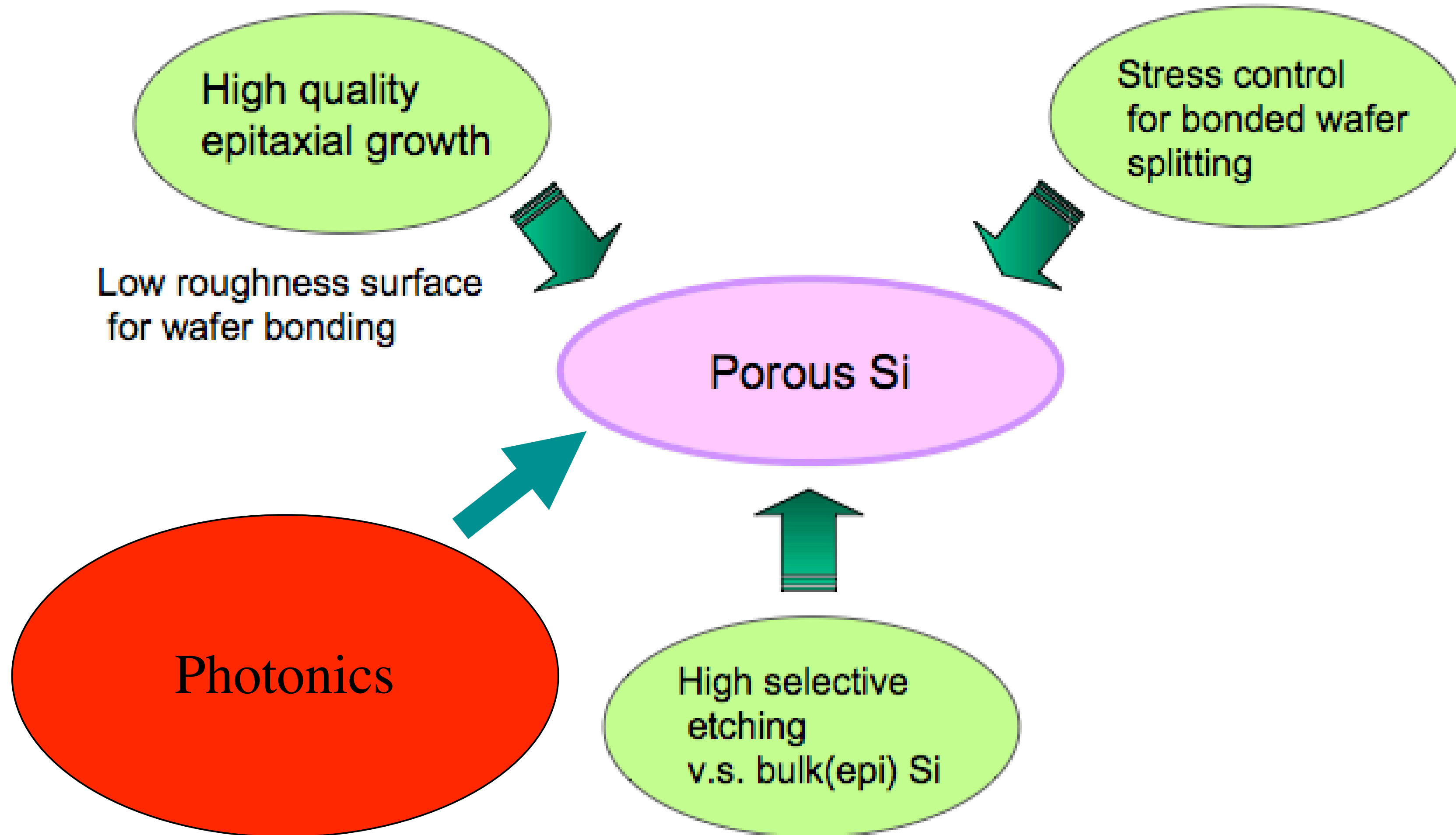
Novel anodization holder & apparatus



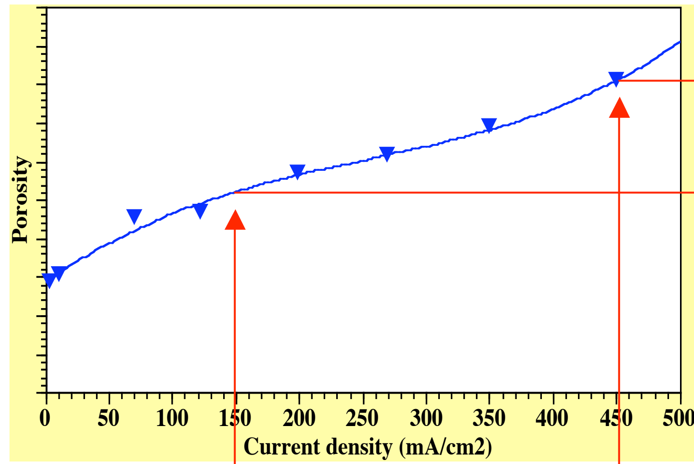
An important role of porous Si in SSTEP

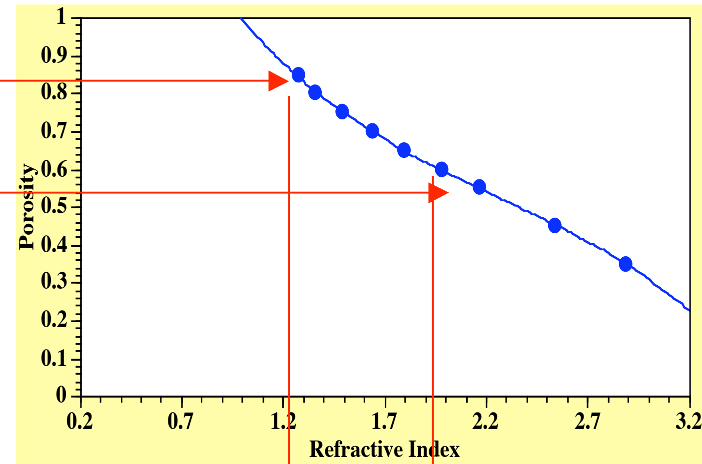


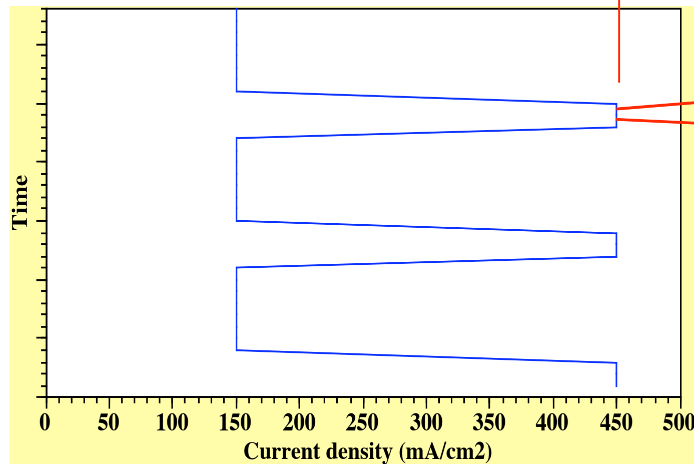
An important role of porous Si in SSTEP



Photonics

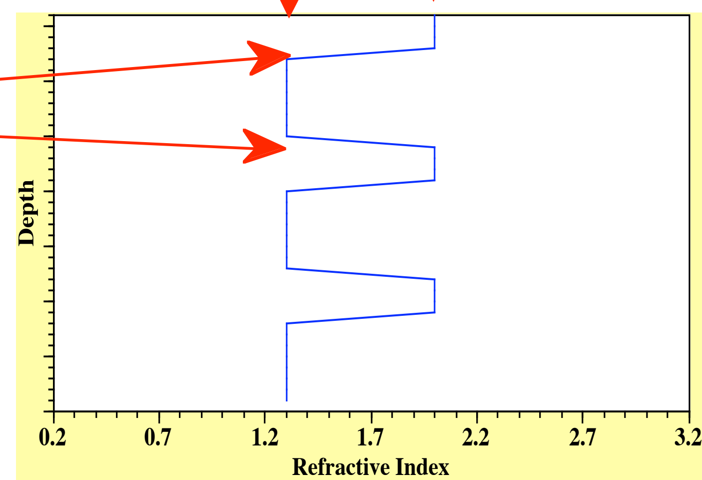




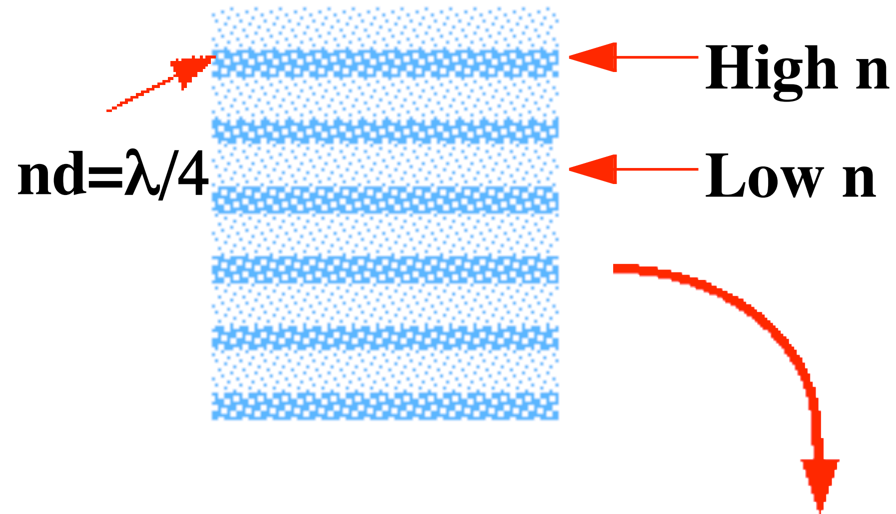


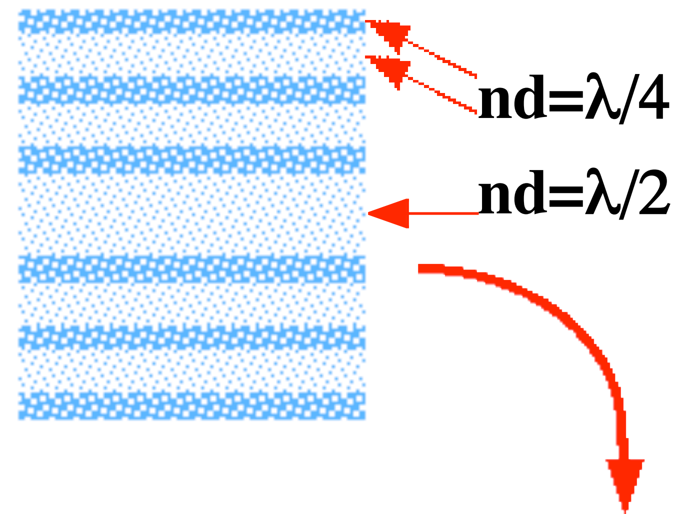
Careful!

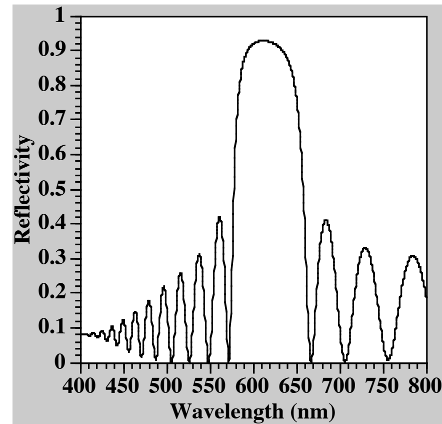
The etch rates are not the same!

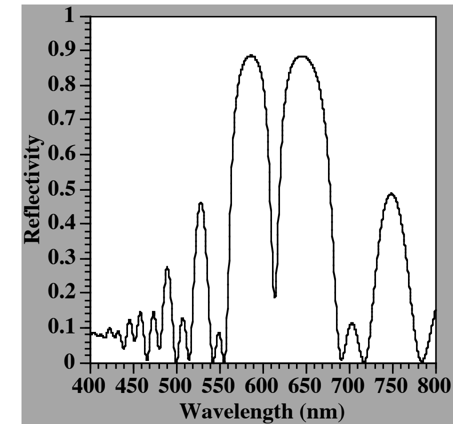


Photonics



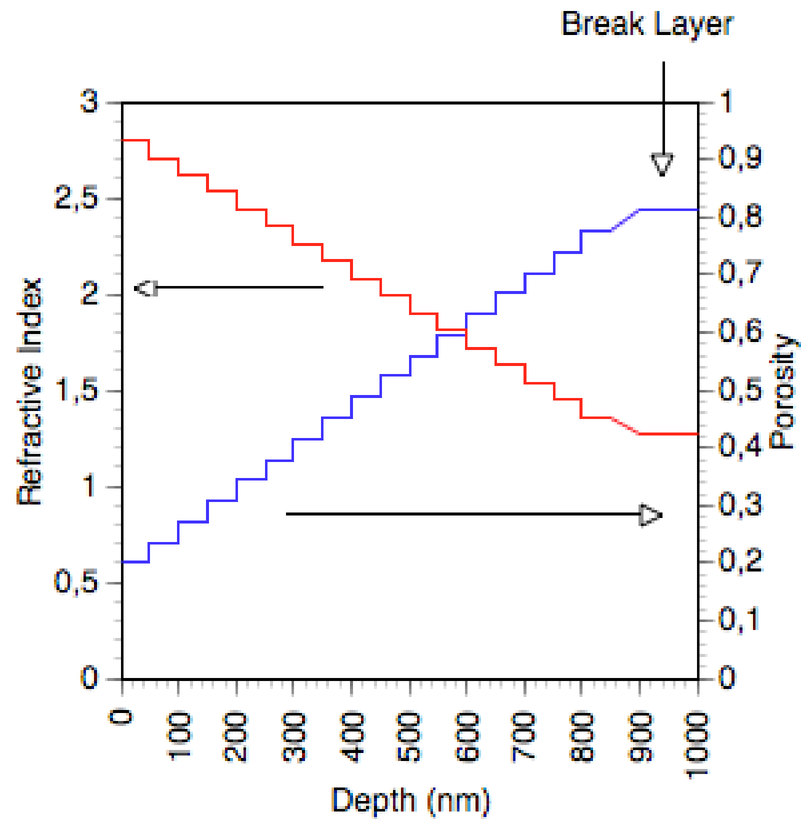


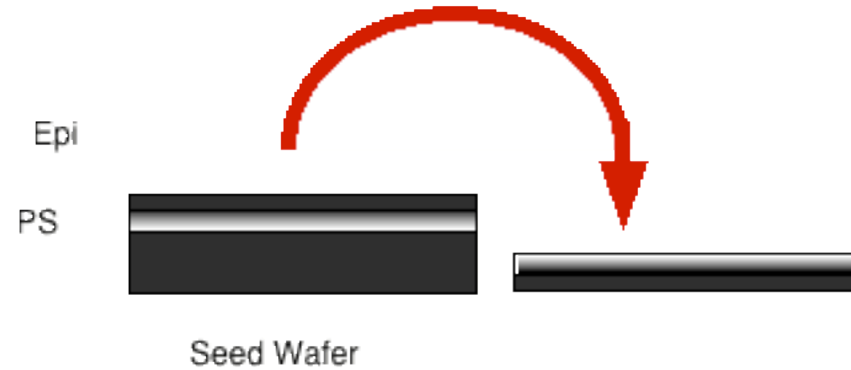




Photonics

Antireflective coating…

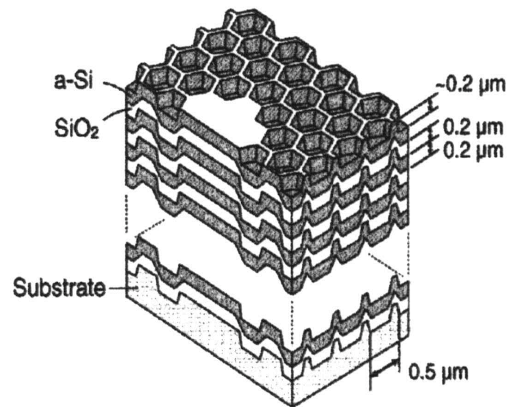




Reducing the index step at the Air-Si interface

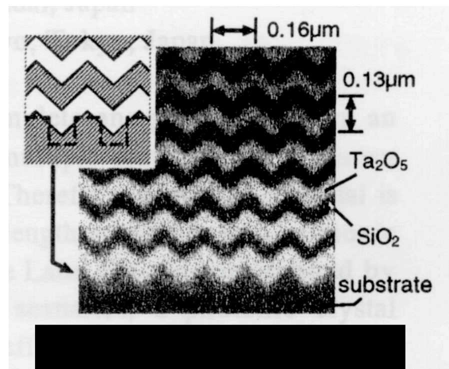
Photonics

Photonic crystals



Obtained using IC's technologies

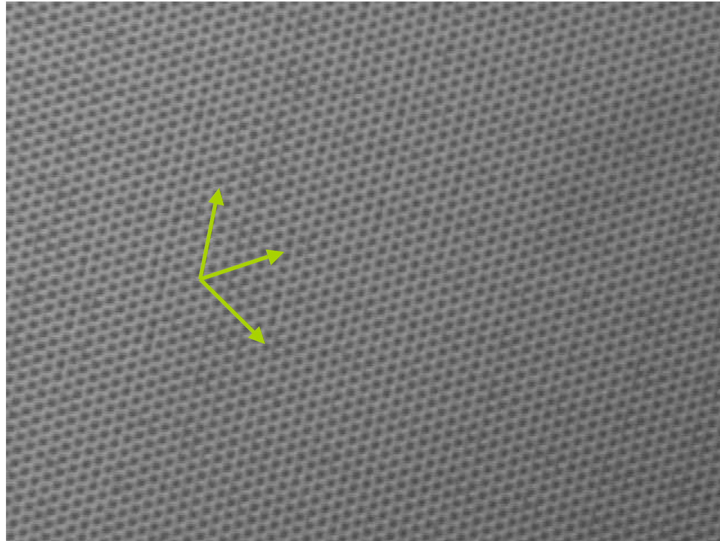
- –Stack of semiconductors stripes
  - **•(asymmetric fcc structure)**
  - •Si (SiO_2)
  - •III-V

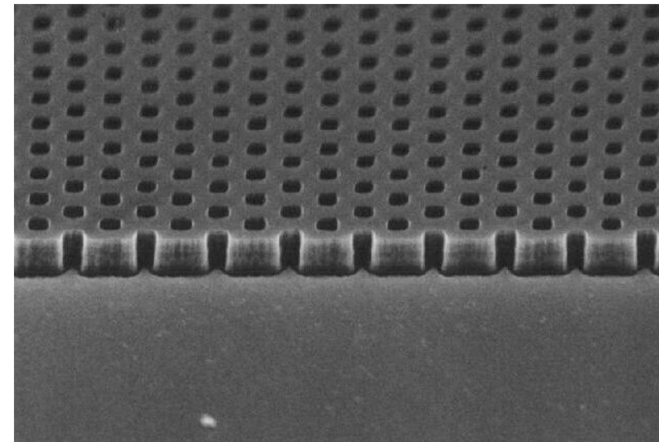


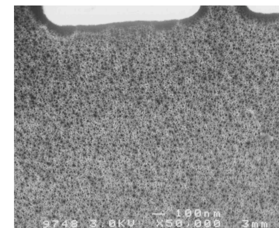
- –Corrugated multilayers

Hanaizumi et al. APL. **74** (1999) http://www-user.riec.tohoku.ac.jp/~pecs/

Photonics

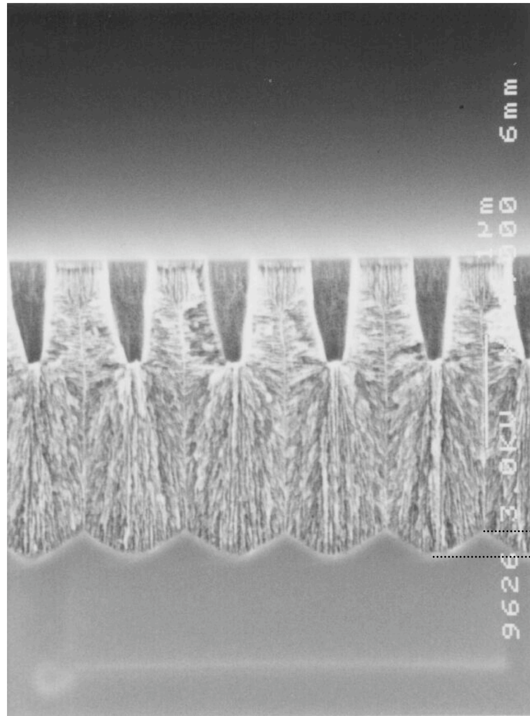






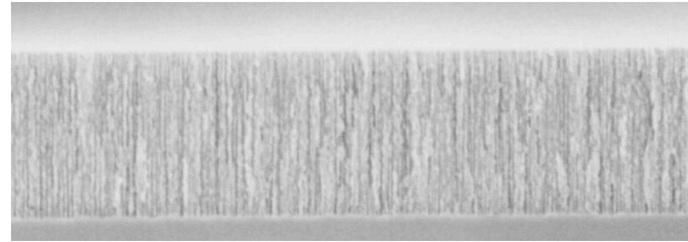
Hexagonal
array of holes (a = 1μm)
obtained by **e-beam lithography**

Photonics

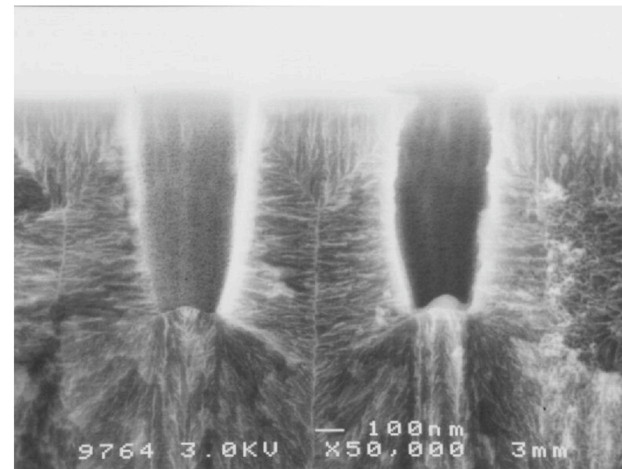


e/2

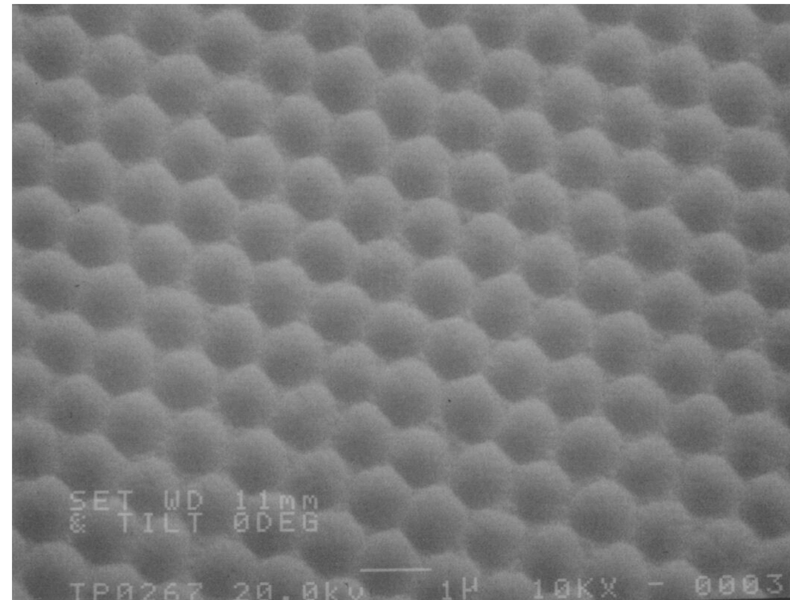
Side view of the patterned area



Side view of the non patterned area

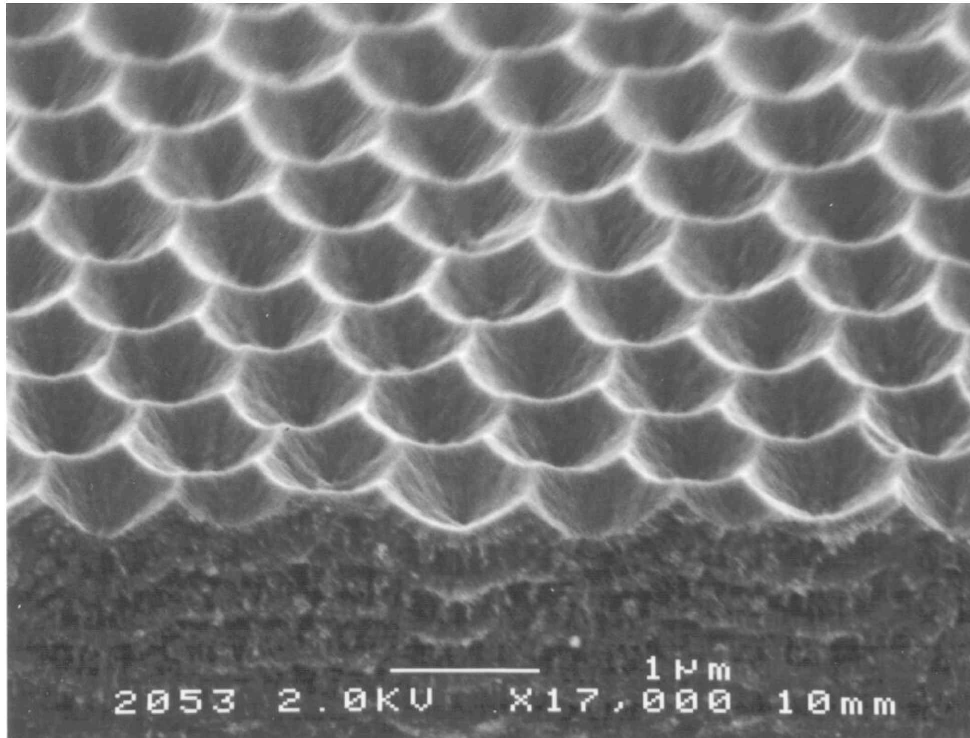


Removal of the layer

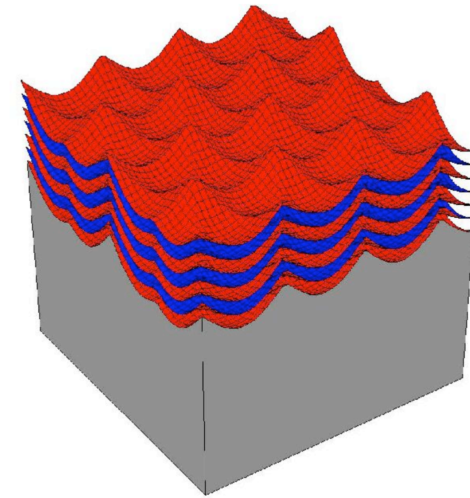


Etching with the current modulation...

Photonics

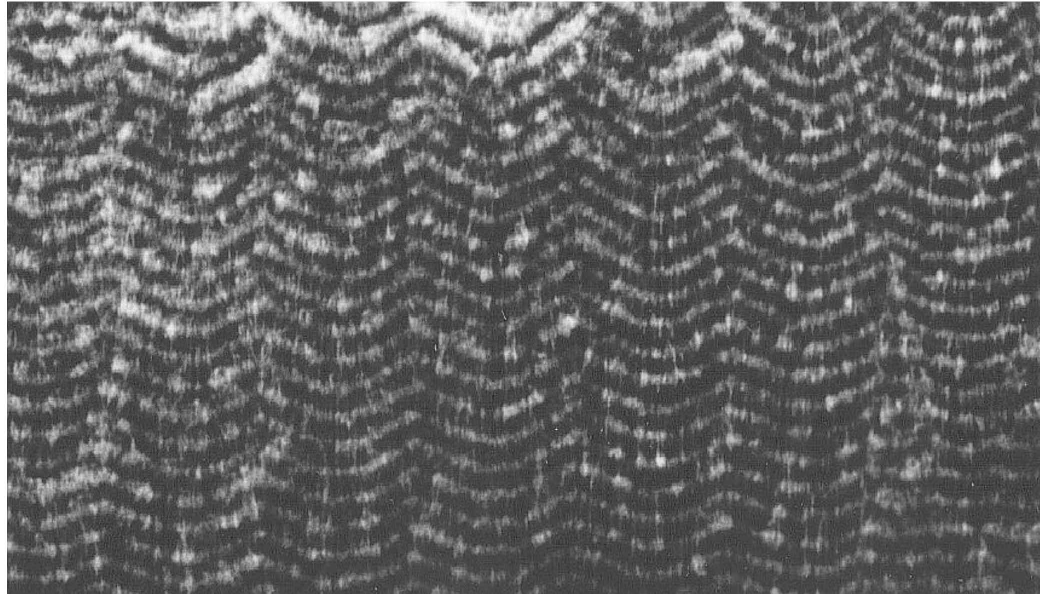


"New wave" Structure



Representation of the refractive index changes

Photonics

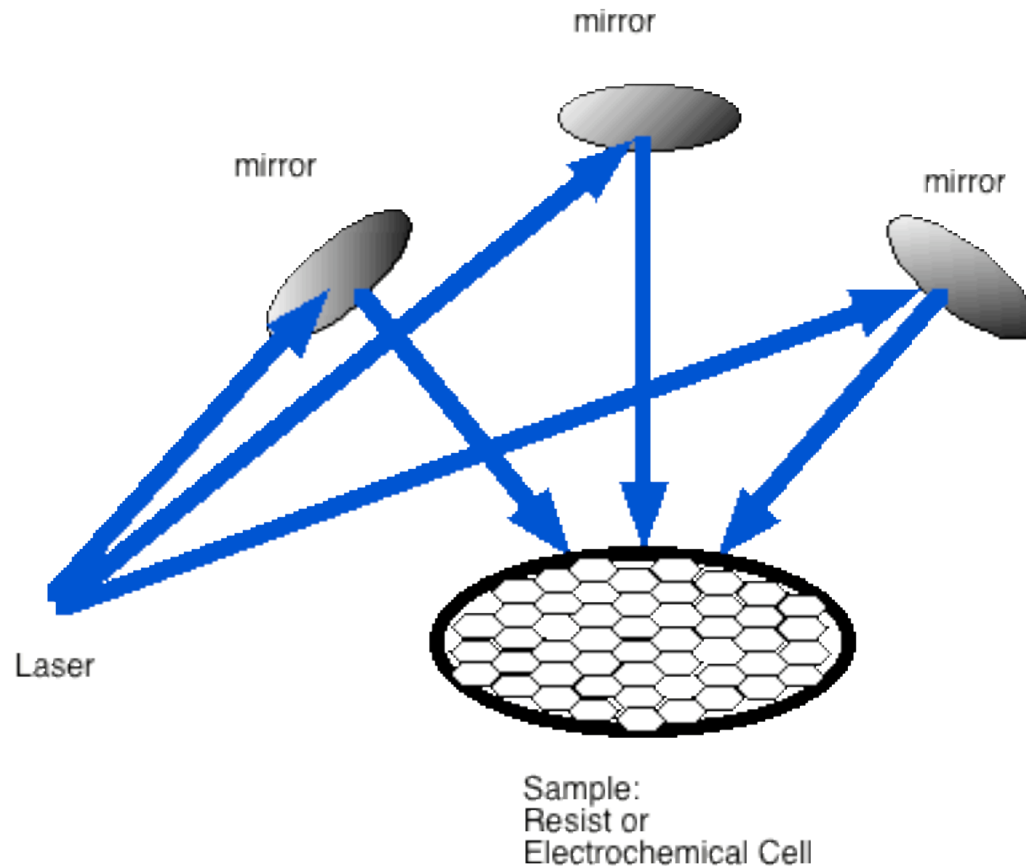


Coherent porosity modulations

No limitation of the number of periods: here 35

Non patterned area

Photonics



3 beam interference

λ= 488 nm

Min period = 244 nm

Conclusions

SSTEP is:

-reliable (it derives from the ELTRAN process)

-flexible ->

- thickness of the Epi-layer
- corrugation of the Epi-layer
- antireflective coatings
- 1D to 3D photonics

-cheap (Y-> R+H)

-needs for financial support (no Martini, no party…)